Development of Microwave Package Models Utilizing On-Wafer Characterization Techniques

Carl Chun, Anh-Vu Pham, Joy Laskar, *Member, IEEE,* and Brian Hutchison

***Abstract*— A package characterization technique using coplanar waveguide (CPW) probes and line–reflect–match (LRM) calibrations for surface-mountable packages is presented. CPW-to-package adapters (CPA) are fabricated on alumina substrates to mount and measure the high-frequency response of plastic packages. Offset CPA standards in conjunction with an LRM calibration are used to de-embed the response of the adapters from the measured S-parameters. Application of this method is demonstrated by characterizing and modeling surface-mount microwave plastic packages.**

***Index Terms*—Calibration, MMIC package, package modeling.**

I. Introduction

THE EMERGING applications of wireless communications require effective low-cost approaches to microwave and RF packaging to meet the demand of the commercial marketplace. Manufacturers are being driven to produce smaller, more efficient, and less expensive electronic components for high-frequency applications. A major determinant of component cost is the package. Surface-mountable packages—especially plastic packages—are a cost-effective solution to low-cost assembly and packaging. However, plastic packages contain unavoidable parasitic elements. As a result, development of characterization techniques for surface-mounted packages is motivated by the need to predict the parasitic behavior of packages at microwave frequencies. Recent work in the literature relies on electromagnetic (EM) simulations and circuit models to predict microwave package behavior [1], [2]. Most recently, time-domain measurements have been used to characterize high-speed digital propagation and to develop equivalent circuit models [3]–[7]. In this paper, we develop an experimental method to measure the S-parameters of surface-mount packages in the frequency domain for the development of high-frequency circuit models. Other approaches to measure surface-mounted packages face two major difficulties: measuring S-parameters in the GHz regime free of resonances contributed by a package test fixture and extracting valid RF frequency-dependent interconnect models from measured characteristics.

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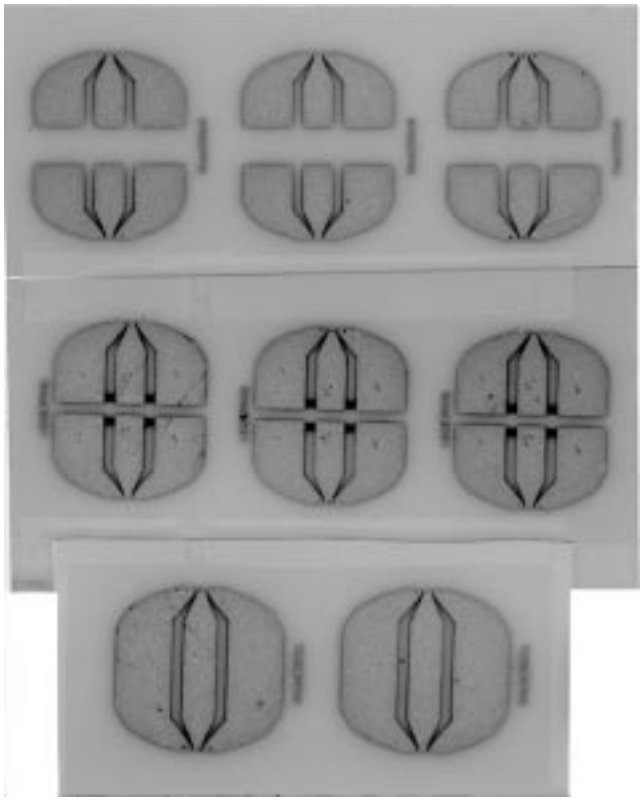

Fig. 1. Offset CPA calibration standards.

In this paper, we present an on-wafer method of measuring the microwave performance of surface-mountable packages. Transition between the on-wafer probes and the package is accomplished via coplanar waveguide (CPW) adapters that connect the probe pads and the package leads. A line–reflect–match (LRM) calibration with offset CPW-to-package adapters (CPA's) is used to shift the measurement reference planes so that only the information of the package under test is acquired. This method is demonstrated by verifying the CPA calibration, showing repeatability of the model, and predicting the response of a packaged monolithic microwave integrated circuit (MMIC) using the package model in a circuit simulator.

II. Calibration and Measurement

In this technique, on-wafer measurements are applied to obtain S-parameters of mounted packages. Lead-frame packages are mounted onto an alumina substrate patterned with CPA's (shown in Fig. 1) enabling measurement with CPW probes

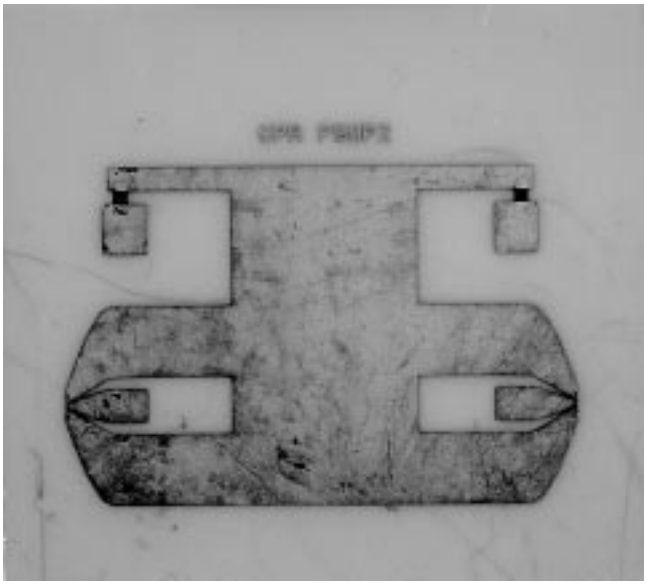

Fig. 2. Alumina substrate patterned for package measurement with CPA's.

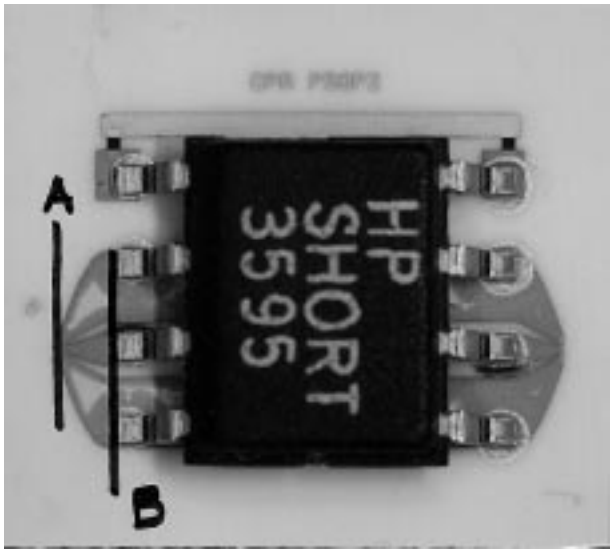

Fig. 3. Package mounted on measurement substrate. (a) Probe reference plane. (b) CPA reference plane.

instead of coaxial fixtures. The CPA's are CPW traces on the alumina substrate that provide a transition between the pitch of the CPW probes used for integrated-circuit (IC) measurements (50–200 μm) and the package pin's (25–50 mil). By modeling this transition as a tapered CPW transmission line between CPW lines of differing geometries, the entire structure is designed to maintain a 50-Ω characteristic impedance.

By establishing the measurement reference plane at the end of the package pin's in the calibration, the adapter response is removed from the measurement. Offset CPA calibration standards (as shown in Fig. 1) are used to perform an LRM calibration. The calibration standards consist of the CPA structures attached to 50-Ω loads, a thru line, and open pads, thereby realizing LRM offset calibration standards. By including the adapters as part of the calibration standards, the measurement reference plane is set to the end of the adapters.

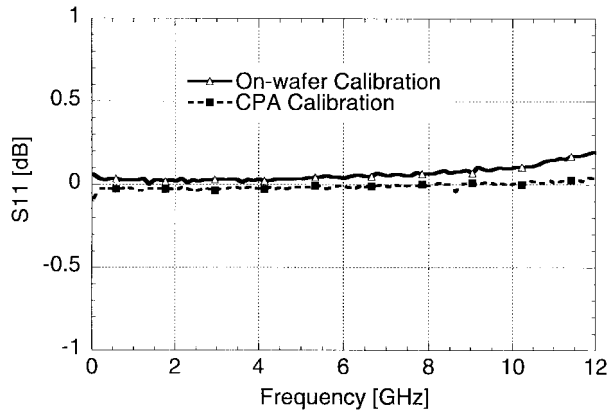

Fig. 4. Comparison of reflection coefficient of a shorted standard from Cascade ISS and CPA substrate.

To measure the electrical characteristics of the package, the package is mounted onto an alumina substrate with CPA's positioned to match the mounting connection of the package, as demonstrated in Fig. 2. An LRM calibration is performed with the offset calibration structures, and then the package is measured with CPW on-wafer probes. After calibration, only the S-parameters of the package are collected. Fig. 3 shows the reference plane at the probe tips (a) and at the end of the CPA (b). When the reference plane is set to point (b), the response of the adapters are de-embedded from the measurement.

To verify the calibration technique, a standard not used in the calibration is measured. The reflection coefficient of a CPA offset short measured with a CPA offset calibration are compared with the reflection coefficient of a Cascade Microtech ISS short measured with an on-wafer LRM calibration, shown in Fig. 4. Since an open is used for the high reflect standard in both calibrations, the measurement of a short (a standard not used in the calibration) provides an indication of the calibration integrity.

III. Experiment

The capability of accurately and easily characterizing packages provides a means to study and correctly model their high-frequency behavior. Measurements of CPA standards are used to develop an equivalent-circuit model for the shrink small-outline package (SSOP) package. The application of this model is demonstrated by comparing the measured results of a packaged on-wafer amplifier with simulations of the equivalent circuit. Measurements of the package were taken with an HP8510C network analyzer and Cascade Microtech CPW probes.

The previously described calibration procedure allows us to collect data which can be used to generate and verify equivalent circuits for the package. Accurate modeling expedites the design process by accounting for parasitic elements during the design of the circuit and predicting the packaged component's characteristics. In this paper, we characterized two plastic packages: an 8-pin small-outline integrated-circuit package (SOIC8) and a 16-pin SSOP (SSOP16), shown in Fig. 5, with dimensions detailed in Table I. The packages were made from plastic housings with lead-frame technology and

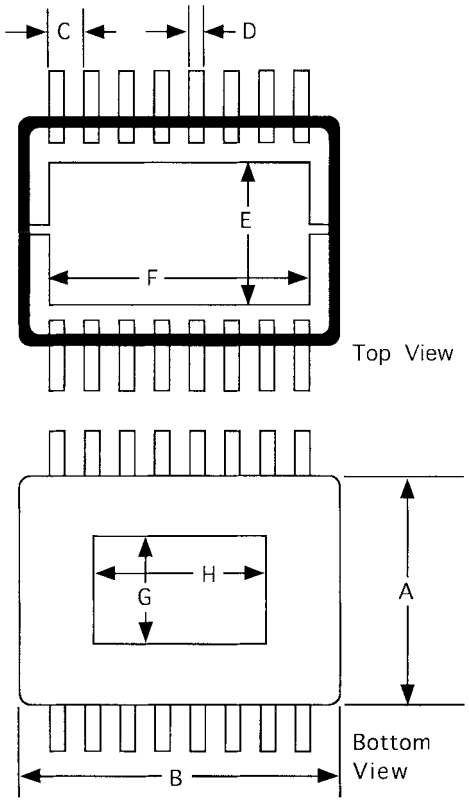

Fig. 5. Package geometry.

TABLE I
PACKAGE DIMENSIONS

	package width (A)	package length (B)	pin pitch (C)	pin width (D)	die pad width (E)	die pad length (F)	heat slug width (G)	heat slug area (H)
SOIC8	0.155"	0.194"	0.050"	0.017"	0.084"	0.120"	0.065"	0.105"
SSOP16	0.155"	0.194"	0.025"	0.010"	0.084"	0.120"	0.065"	0.105"

gull-wing pins. The heat slug which extends from the die pad inside the package to the mounting substrate provides a ground plane as well as a thermal path to the substrate or printed circuit board (PCB).

Grounded coplanar standards (50-Ω load, short, thru line, and open) are fabricated on 125-μm-thick sapphire substrates. These passive structures are measured with on-wafer CPW probes using an LRM calibration on a Cascade Microtech impedance standard substrate (ISS), thereby generating a two-port S-parameter model of each structure. These structures are mounted onto the copper die pad of the packages with conductive epoxy. Wirebonds attach the lead frame to the probing pads of the passive structures in a three-wire ground–signal–ground (GSG) configuration. An example of a 50-Ω structure mounted in a package is shown in Fig. 6. The open cavity of the package is then encapsulated with hysol, and the entire package is mounted onto an alumina substrate patterned, as shown in Fig. 3. The pattern connects the ground of the CPW probes with the ground slug of the package. The pattern is dependent on the use of the pins. A CPW input is assumed in this paper, but this technique can

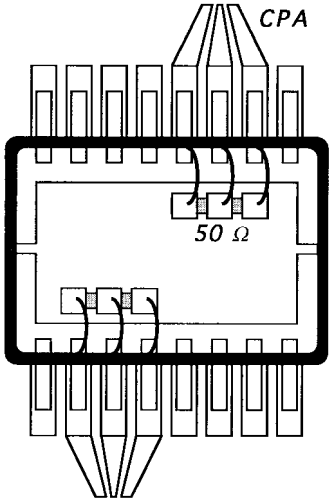

Fig. 6. On-wafer 50-Ω standard mounted in package.

TABLE II
EQUIVALENT CIRCUIT MODEL OF PLASTIC PACKAGES

Package	Pin inductance: pin	Capacitance to ground: C_g	Resistance to ground: R_g	Capacitance between pins: C1	Paddle inductance: slug
SOIC8	0.74 nH	0.16 pF	10 Ω	0.085 pF	0.021 nH
SSOP16	0.85 nH	0.22 pF	3.7 Ω	0.22 pF	0.022 nH

be extended to include other feed configurations. A microstrip feed, commonly used in PCB's, can be accommodated by adapting a coplanar feed to a microstrip line in a manner demonstrated by Pham *et al.* [8].

An LRM calibration is made with the CPA offset standards, and each of the packaged standards are measured with the technique described to acquire the S-parameters of the entire package. An equivalent circuit based on existing models for similar geometry structures is chosen for the package. It should be noted that the equivalent circuit need not be unique and the model used in this investigation is just one suggestion. The model and the measured S-parameters of the on-wafer standards are combined to generate models of the packaged standard. These models are fitted to the measured data by optimizing the parasitic elements of the model in Hewlett-Packard's Microwave Design System (MDS). As needed, the equivalent circuit is modified to accommodate the specific configuration of the signal feed.

The topology of the equivalent circuit is based on models used for SOIC8 packages [1], [2] and the configuration of the CPW signal input/output (I/O) in our measurement. The plastic package used in this paper differs from those previously studied [1], [2]. The ground paddle of the package in this paper extends to the bottom of the package to provide a thermal and electrical path to the mounting substrate; therefore, the modeling of the image current behavior demonstrated by Jackson [2] is not necessary here. The model topology is simplified by removing the effects of mutual inductance between leads and capacitive coupling between nonadjacent pins. In the arrangement of the package in this paper, the

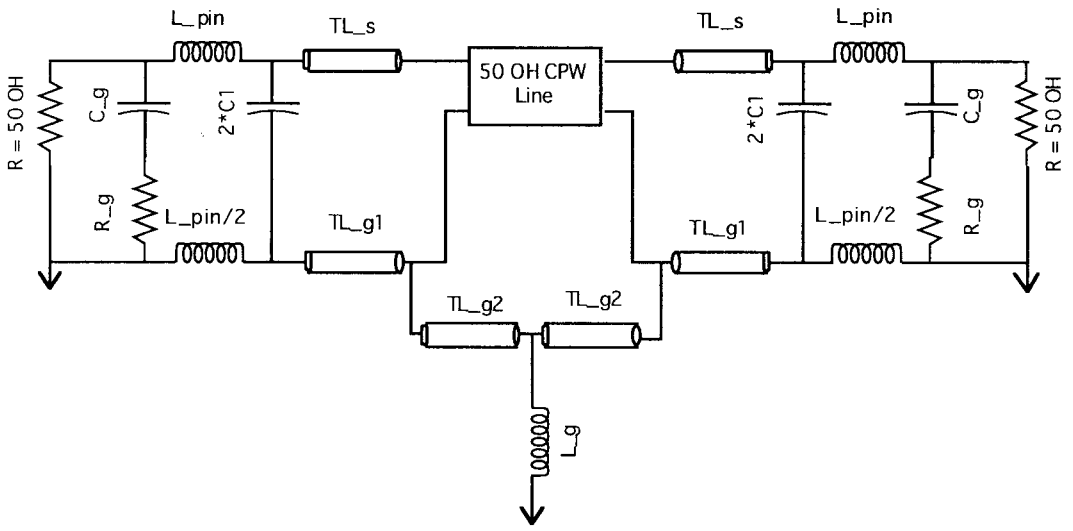

Fig. 7. Equivalent circuit for packaged CPW standards.

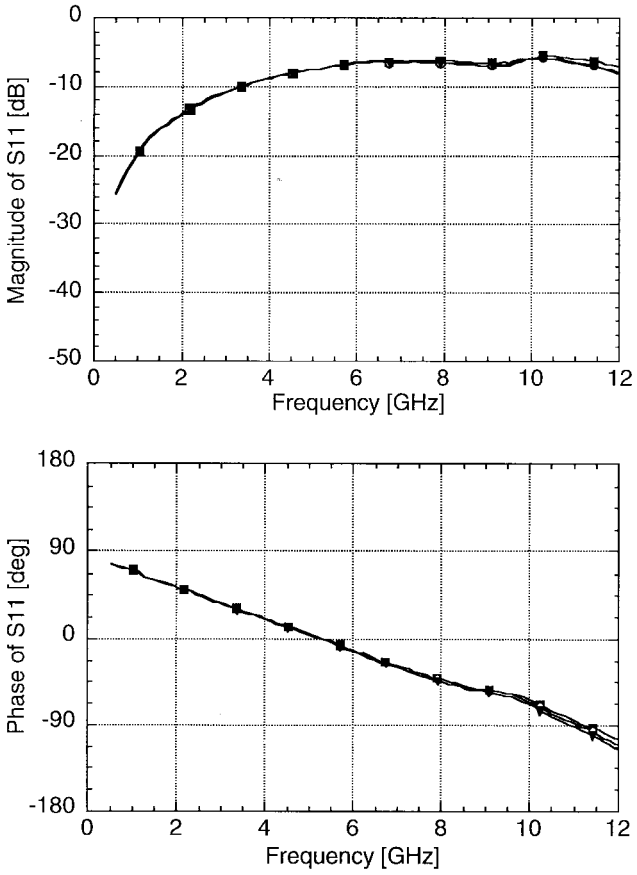

Fig. 8. Comparison of measured S_{11} of three packaged thru lines.

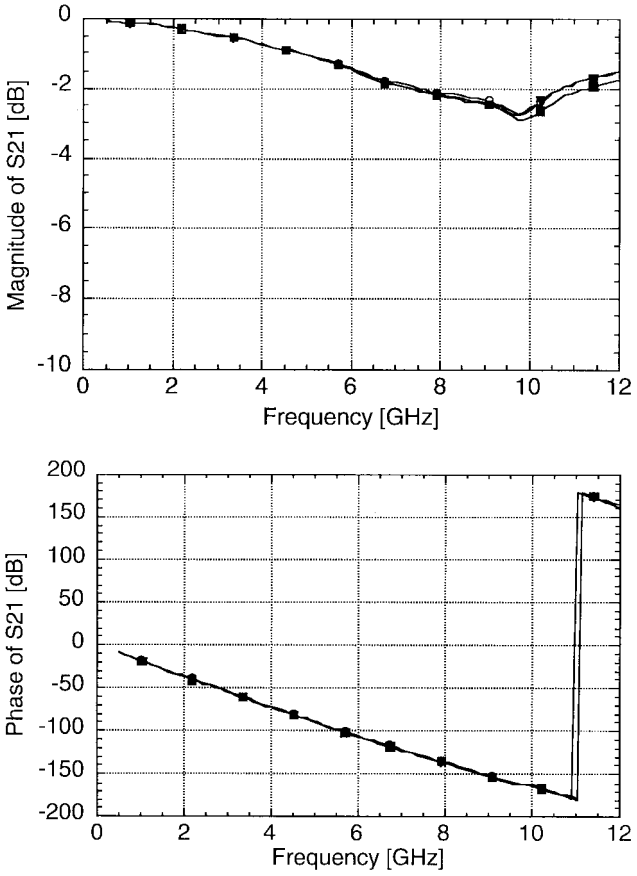

Fig. 9. Comparison of measured S_{21} of three packaged thru lines.

mutual inductance from the signal path to the two surrounding ground pins is assumed to be negligible because the GSG input approximates a transmission-line feed. The model is further modified by including a resistance and capacitance to ground to provide a better fit to measured data. Three basic components (the leads, the coupling of the leads, and the ground plane) are put together to form the pseudo-physical model. The model used for our measurement configuration of the grounded CPW standards is shown in Fig. 7. The parasitics of the lead are modeled as an inductance, L_pin. The capacitor $C1$ connected between the pins models the coupling between adjacent pins. The inductance associated with the ground plane is represented by the inductor L_g. For an improved parasitic model, a capacitance, C_g, in series with a small resistance, R_g, is shunted across the signal pin to ground. Since the bondwires are no longer surrounded by air, the bondwires are

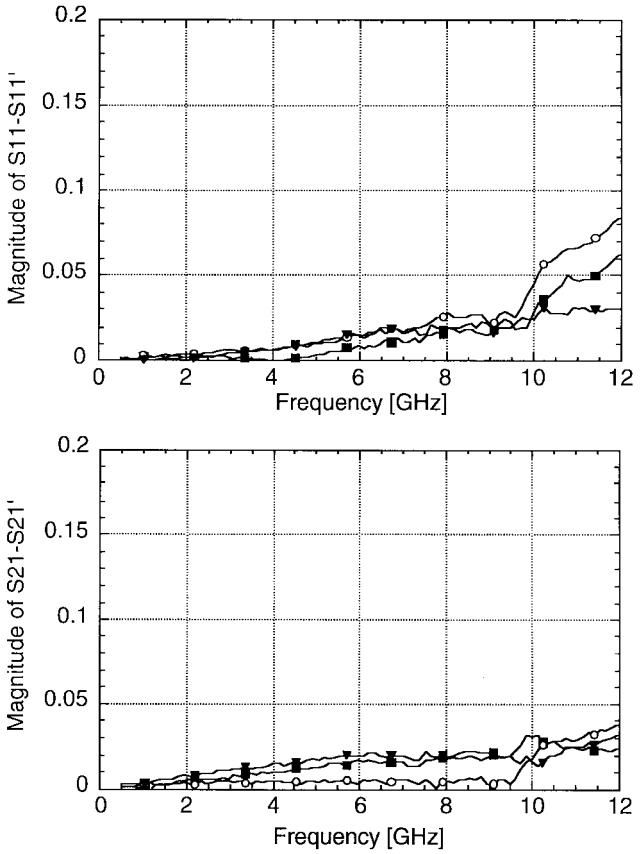

Fig. 10. Difference in measured S-parameters of thru lines.

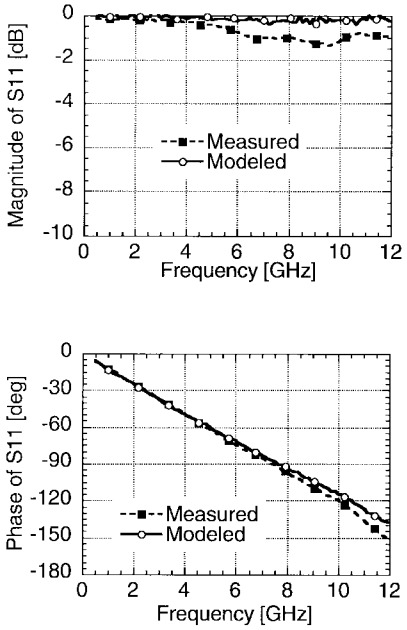

Fig. 11. Comparison of measured S_{11} of open standard packaged in SSOP16 and simulated S_{11} of open standard in SSOP16 model.

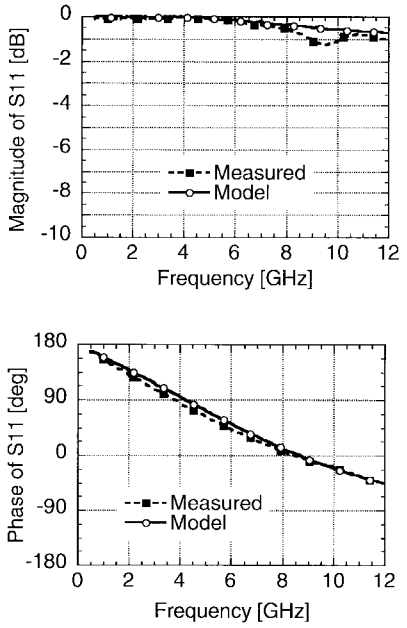

Fig. 12. Comparison of measured S_{11} of short standard packaged in SSOP16 and simulated S_{11} of short standard in SSOP16 model.

replaced with transmission lines and are optimized with the parasitic parameters of the equivalent circuit. Because of the GSG configuration of the CPW probes, there are two ground paths, each with parasitic elements (L_pin, $C1$, TL_g1). Since these two paths are identical and in parallel, they are combined together to form a single path and the corresponding model values are adjusted accordingly. The ground pads of the passive standards are also wirebonded to the slug of the package, which is represented in the equivalent circuit by the transmission lines labeled TL_g2. Conventional models of a bondwire are not used because the inherent assumption of air surrounding the wire is incorrect for the encapsulated package. The characteristic impedance of the bondwires needs to be optimized because the encapsulating epoxy affects the bondwire's characteristic response; however the bondwire lengths are constrained to the physical dimensions of the actual bondwire to isolate the effect of our epoxied bondwire model from that of the package model.

Optimized values of the package parasitic elements have been determined for both the SOIC8 and SSOP16, as shown in Table II. The similar parasitic values reflect the fact that these two packages posses the same basic geometry. Capacitance between pins is increased in the SSOP16 package due to the smaller pitch between the leads, while the remaining component values are comparable.

In the case of the SSOP16, 50-Ω load, short, open, and thru standards are used to generate the equivalent-circuit values. Each standard is assembled in three packages to help remove any deviations caused by reliability of package placement and connection. Figs. 8–9 show the reflection and insertion loss of three different packaged thru lines. By taking the magnitude of the difference in S-parameters of the three measured packages, the typical deviation of the different measurements is quantified and shown in Fig. 10. The typical difference in magnitude for all the standards is about 0.05 with none greater than 0.1 in this paper. To demonstrate the validity of the model, the measured S-parameters of packaged standards are shown with the simulated S-parameters of packaged standards in Figs. 11–15. When the measured and modeled S-parameters are compared, close fits are shown for the cases of

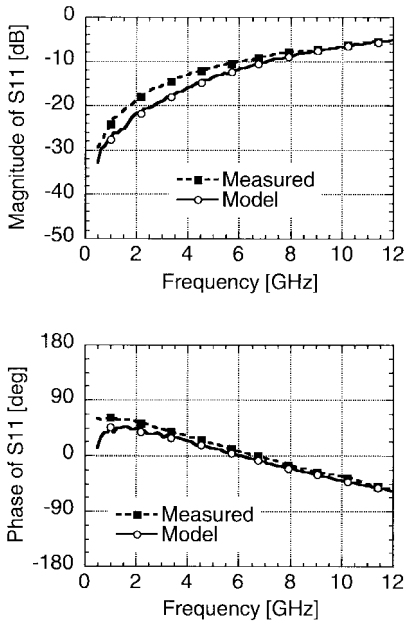

Fig. 13. Comparison of measured S_{11} of load standard packaged in SSOP16 and simulated S_{-11} of load standard in SSOP16 model.

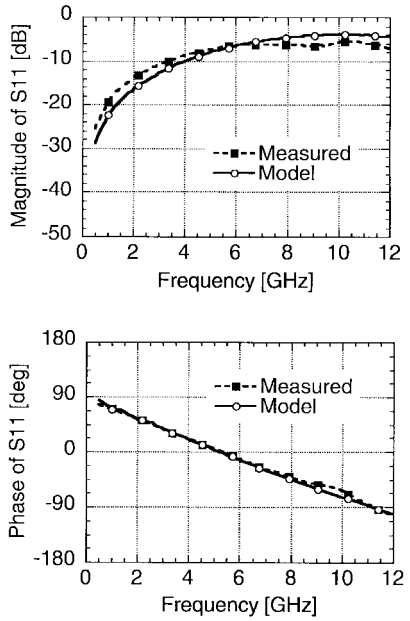

Fig. 14. Comparison of measured S_{11} of thru standard packaged in SSOP16 and simulated S_{11} of thru standard in SSOP16 model.

the packaged open, short, load, and thru standards, showing applicability to a range of impedances.

As a demonstration of the usefulness of this electrical model, the characteristics of a packaged amplifier is predicted. A two-stage heterojunction bipolar transistor (HBT) GaAs MMIC amplifier is used to validate the developed package model. The circuit model of an unpackaged HBT amplifier is incorporated with the package model to simulate the characteristics of the packaged amplifier. Unpackaged, the amplifier circuit shows a 3-dB cutoff frequency of greater than 15 GHz, but packaging the chip reduces the cutoff frequency to about 8 GHz. The amplifier is wirebonded into an SSOP16 package and measured with CPA's on alumina and CPW probes to

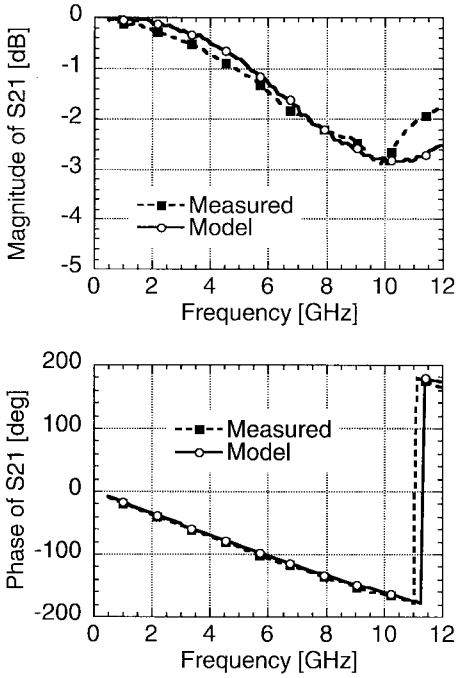

Fig. 15. Comparison of measured S_{21} of thru standard packaged in SSOP16 and simulated S_{21} of thru standard in SSOP16 model.

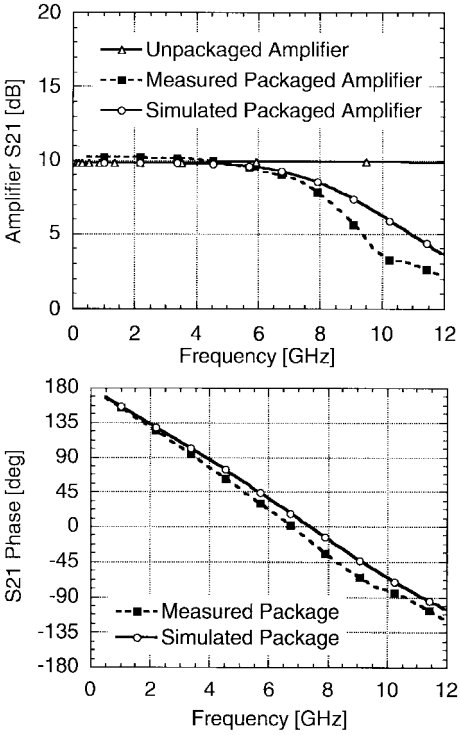

Fig. 16. Comparison of measured and modeled S_{21} of amplifier.

substantiate the predicted results. The gain of the simulated unpackaged, simulated packaged, and the measured packaged amplifier are compared in Fig. 16, and confirm the usefulness of the model.

IV. Conclusion

A new technique for on-wafer measurement of surface-mountable packages has been developed. This technique can

be generalized to characterize surface-mount packages into the gigahertz range. By using offset CPA calibration standards and calibrating to the ends of the package leads, only the response of the package were gathered, and resonant-free measurements of the high-frequency electrical performance of plastic packages have been demonstrated by comparing CPA standards measured with a CPA calibration substrate and CPW standards measured with an on-wafer LRM substrate. A DC-12-GHz model of the package has been generated from measured data and validated with experimental results of an amplifier test vehicle. Simulated S-parameters of a packaged amplifier correctly predicted the measured results allowing circuit designers to compensate for package parasitics during design. Although the package model presented here is a pseudo-physical model, it serves the purpose of a simple equivalent circuit useful for determining the response of a packaged component in circuit simulations. Other models can be generated with this measurement approach that are suitable for each specific need.

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